UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/875,855 | 06/08/2001 | Kinya Osa | 862.C2255 | 9364 |

5514 7590 07/02/2004

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

| EXAMINER | |
|---|---|
| LAROSE, COLIN M | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2623 | |

DATE MAILED: 07/02/2004

5

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/875,855 | OSA, KINYA | |
| | Examiner | Art Unit | |
| | Colin M. LaRose | 2623 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 4 and 11 are objected to because of the following informalities:

"specifying a non-zero highest-order bit potion" should be -- specifying a non-zero highest-order bit position --. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,266,450 by Yip et al. ("Yip").

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 8, Yip discloses an apparatus and method (figure 3) for outputting a data group (i.e. coefficients of image data) having data represented by plural bits to predetermined processing means (i.e. coding routine 314), comprising:

detection means for detecting a maximum value in the data group as a transfer object (306 and column 6, lines 66-67: the largest coefficient in the data group is identified); and

specifying means for specifying a non-zero highest-order bit position among bits constructing the maximum value detected by said detection means (306 and column 6, lines 66-67: the MSB bit position (i.e. the highest significant bitplane) of the maximum detected value is specified as "maxBitNumber"),

wherein a bit in a position higher than said highest-order bit position specified by said specifying means is omitted from processing by said predetermined processing means (Figure 4 shows the "Code region" routine of figure 3. As can be seen in figure 4, coding begins with the "maxBitNumber" bitplane and continues until the "minBitNumber" bitplane is reached. As a result, those bits in the bitplanes higher than the "maxBitNumber" bitplane are omitted from processing.)

Regarding claim 5, Yip discloses the predetermined processing means is a coding processor circuit (314, figure 3).

Regarding claims 6 and 12, Yip discloses including any known memory circuit, which includes a DMA circuit (column 23, lines 53-57).

Regarding claim 7, Yip discloses the data group includes transform coefficients generated by transform coding on the pixel data (304, figure 3).

Regarding claims 2 and 9, Yip discloses an apparatus and method (figure 3) for outputting a data group (i.e. coefficients of image data) having data represented by plural bits to predetermined processing means (i.e. coding routine 314), comprising:

calculation means for performing logical OR calculation on all the data group to be transferred (306 and column 6, lines 66-67: the largest coefficient in the data group is identified; figure 29, and column 19, line 58 through column 20, line 10: the "bit-plane unit" in figure 29 performs a logical OR operation on all the bits in a current bit plane and the previous bit planes in order to generate "data valid bits,"); and

specifying means for specifying a non-zero highest-order bit position among bits constructing the result of the logical OR calculation by said calculation means (306 and column 6, lines 66-67: the MSB bit position (i.e. the highest significant bitplane) of the maximum detected value is specified as "maxBitNumber"; and column 20, lines 25-31: the data valid bits are used for determining the most significant data bit),

wherein a bit in a position higher than said highest-order bit position specified by said specifying means is omitted from processing by said predetermined processing means (Figure 4 shows the "Code region" routine of figure 3. As can be seen in figure 4, coding begins with the "maxBitNumber" bitplane and continues until the "minBitNumber" bitplane is reached. As a result, those bits in the bitplanes higher than the "maxBitNumber" bitplane are omitted from processing.)

Regarding claims 3 and 10, Yip discloses an apparatus and method (figure 3) for outputting a data group (i.e. bitplanes of coefficients) having data represented by plural bits to predetermined processing means (i.e. coding routine 314), comprising:

calculation means for performing logical OR calculation on all the data group to be transferred (figure 29, and column 19, line 58 through column 20, line 10: the "bit-plane unit" in figure 29 performs a logical OR operation on all the bits in a current bit plane and the previous bit planes in order to generate "data valid bits,"); and

specifying means for specifying a non-zero lowest-order bit position among bits constructing the result of the logical OR calculation by said calculation means (see column 7, lines 8-13: a non-zero lowest-order bit position, corresponding to the "minBitNumber" bitplane, is designated according to the desired image quality; and Yip's lowest-order bit position is "among bits constructing the result of the logical OR calculation" – since all bits in bitplanes lower than the maxBitNumber bitplane are used to construct the results of the logical OR calculation in column 20, the designated lowest-order bitplane ("minBitNumber") comprises bits used to construct the results of the logical OR calculation),

wherein a bit in a position lower than said lowest-order bit position specified by said specifying means is omitted from processing by said predetermined processing means (Figure 4 shows the "Code region" routine of figure 3. As can be seen in figure 4, coding begins with the "maxBitNumber" bitplane and continues until the "minBitNumber" bitplane is reached. As a result, those bits in the bitplanes lower than the "minBitNumber" plane are omitted from processing.)

Regarding claims 4 and 11, it is noted that claim 4 is a combination of claims 2 and 3, and claim 11 is a combination of claims 9 and 10, the features of claims 2, 3, 9, and 10 being fully disclosed by Yip as recited above.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 6,208,761 by Passaggio et al.

U.S. Patent 5,442,458 by Rabbani et al.

U.S. Patent 6,658,159 by Taubman

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colin M. LaRose whose telephone number is (703) 306-3489. The examiner can normally be reached Monday through Thursday from 8:00 to 5:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au, can be reached on (703) 308-6604. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2600 Customer Service Office whose telephone number is (703) 306-0377.

CML

Group Art Unit 2623

17 June 2004

AMELIA M. AU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600